Language: English
Abstract: Development of the high performance parallel computer systems suffers today from lack of the software that would allow simple programming with consequent optimal and safe program execution. The main goal of the research for this scope is to provide a programming environment that allows application programmers to develop parallel programs without worrying about the physical machine they are programming. The problem of balanced parallel program allocation onto distributed-memory message-passing parallel systems (multicomputers) can be solved by using problem-solving methods of the artificial intelligence. Our method proposed also includes communication approach for optimal and safe traffic. We implemented this method as a software tool for automatic configuration of parallel programs in transputer environment.
Subfile: C

3/AB,3/28 (Item 28 from file: 2)
DIALOG(R)File 2:INSPEC

5211097 INSPEC Abstract Number: B9604-6210L-085, C9604-5620L-043
Title: "Fast Ethernet" gets plug-and-play
Author(s): Crayford, I.
Author Affiliation: I/O & Network Products Div., Adv. Micro Devices Inc., Sunnyvale, CA, USA
Conference Title: WESCON/95 Conference Record (Cat. No.95CH35791) p. 354-9
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA xi+778 pp.
ISBN: 0 7803 2636 9 Material Identity Number: XX93-01857
Conference Title: Proceedings of WESCON`95
Conference Sponsor: IEEE; ERA
Conference Date: 7-9 Nov. 1995 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The IEEE 802.3 "Fast Ethernet" standard implements an "auto-negotiation" mechanism which allows any existing or future Ethernet LAN using an RJ-45 connector and unshielded twisted pair cable to simply "plug and play". The mechanism is designed to ensure interoperability between the variety of standards based Ethernet networks, including existing 10 Mb/s devices, and new 100 Mb/s half duplex and full duplex capable devices. Automatic configuration occurs without user intervention, and will negotiate the optimal mode at which the devices at both ends of a link can commonly operate. In the event the devices share no common mode, the auto-negotiation scheme ensures that operation of the rest of the network is not disrupted, and allows the absence of a shared operational mode to be reported via network management. The paper examines the key aspects of the technology surrounding the auto-negotiation scheme, as well as specific examples of the use of the auto-negotiation approach and how it solves potential interoperability problems.
Subfile: B C

3/AB,3/29 (Item 29 from file: 2)
DIALOG(R)File 2:INSPEC

5164883 INSPEC Abstract Number: C9603-5610P-002
Title: A Fujitsu single-chip controller for the plug-end-play environment
Author(s): Spinelli, A.

options. Intermediate results and processing parameters are readily accessible through the friendly user-interface supporting input, output, display and hardcopy of signals or images in various formats on DOS compatible media or Exabyte tape.
Subfile: A B C

3/AB,3/33 (Item 33 from file: 2)
DIALOG(R)File 2:INSPEC

4712121
Title: Plug and play is almost here (automatic PC configuration)
Author(s): Ristelhueber, R.
Journal: Electronic Business Buyer vol.20, no.5 p.43-4
Publication Date: May 1994 Country of Publication: USA
CODEN: EBBUEK ISSN: 0163-6197
Language: English
Abstract: Automatic configuration of user-modified PCs will dramatically expand the market for add-in sound cards, disk drives, and other components. The plug-and-play (PnP) series of hardware and software elements will permit users to simply insert a card or peripheral into a desktop system and have it start running immediately, without a lot of fussing and fuming. In about a year (1995), the key standards and specifications will be in place to make PnP a reality.
Subfile: D

3/AB,3/34 (Item 34 from file: 2)
DIALOG(R)File 2:INSPEC

4658384 INSPEC Abstract Number: C9406-6110P-025
Title: Automatic configuration and optimization of parallel transputer applications
Author(s): Mitschele-Thiel, A.
Author Affiliation: Erlangen-Nurnberg Univ., Germany
p.1052-67
Editor(s): Grebe, R.; Hektor, J.; Hilton, S.C.; Jane, M.R.; Welch, P.H.
Publisher: IOS Press, Amsterdam, Netherlands
Publication Date: 1993 Country of Publication: Netherlands 1317 pp.
Conference Title: Proceedings of the 1993 World Transputer Congress. Transputer Applications and Systems '93
Conference Date: 20-22 Sept. 1993 Conference Location: Aachen, Germany
Language: English
Abstract: The described programming environment represents an integrated approach to automate system design and implementation of transputer applications. The programming environment consists of a programming language and an integrated set of tools. The modeling tool automatically derives a software model from the given application program. Based on the software model and additional optimization guidelines, the model-based optimization computes the design decisions as the network topology, the task granularity, the task assignment and their execution order. Finally, the compiler/optimizer transforms the application program into executable code for the chosen transputer network reflecting the design decisions. Our major achievements concern the integration of model-based performance optimization with program transformation techniques to generate optimized parallel applications. This includes the extension of optimal compile-time scheduling algorithms to integrate the optimization of the network topology. In addition, the software model that can be handled by the algorithm allows conjunctive and disjunctive program structures.
Subfile: C

flexible in both functionality and control, allowing a range of modules and control architectures to be used without modification of modules. This flexibility must be supported by a modelling strategy which allows specification of a module's functionality, and a well-defined mechanism for combining modules. This paper presents a sensor-oriented functional model of modular robotics systems. We describe our approach to modelling robotics resources, which uses semantic annotations to enhance the specification of functionality. A mechanism which successfully detects and resolves consequences of module combination is described, and results from our implementation of this mechanism presented. We outline the application of this work to the automatic configuration of varying control architectures without modification of modules or additional burden on the operator.
Subfile: C

3/AB,3/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

5954092 INSPEC Abstract Number: C9808-5440-008
Title: Automatic configuration of embedded multicomputer systems
Author(s): Beck, J.E.; Siewiorek, D.P.
Author Affiliation: Delco Electron. Corp., Kokomo, IN, USA
Journal: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol.17, no.2 p.84-95
Publisher: IEEE,
Publication Date: Feb. 1998 Country of Publication: USA
CODEN: ITCSDI ISSN: 0278-0070
SICI: 0278-0070(199802)17:2L.84:ACEM;1-E
Material Identity Number: B959-98008
U.S. Copyright Clearance Center Code: 0278-0070/98/$10.00
Language: English
Abstract: This paper considers the problem of automatically configuring multicomputers for use in embedded applications. The configuration problem is decomposed into two subproblems: (1) specification of the hardware components and (2) assignment of the software tasks to the hardware. An automated technique is introduced to solve these subproblems concurrently. The technique is described and then verified on a set of real and synthetic test cases. The paper concludes with a discussion and summary of the results.
Subfile: C

3/AB,3/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

5939860 INSPEC Abstract Number: C9807-6115-024
Title: Achieving middleware customization in a configuration-based development environment: experience with the Aster prototype
Author(s): Issarny, V.; Bidan, C.; Saridakis, T.
Author Affiliation: IRISA/INRIA, Rennes, France
Conference Title: Proceedings. Fourth International Conference on Configurable Distributed Systems (Cat. No.98EX159) p.207-14
Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 1998 Country of Publication: USA viii+233 pp.
ISBN: 0 8186 8451 8 Material Identity Number: XX98-01299
U.S. Copyright Clearance Center Code: 0 8186 8451 8/98/$10.00
Conference Title: Proceedings. Fourth International Conference on Configurable Distributed Systems (Cat. No.98EX159)

Title: Understanding Universal Serial Bus. 1. USB basics
Author(s): Canosa, J.
Journal: Embedded Systems Programming vol.10, no.6 p.34-6, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58
Publisher: Miller Freeman,
Publication Date: June 1997 Country of Publication: USA
CODEN: EYPRE4 ISSN: 1040-3272
SICI: 1040-3272(199706)10:6L.34:UUSB;1-S
Material Identity Number: 0692-97006
Language: English
Abstract: Connectivity is a big issue for embedded systems today, and the Universal Serial Bus (USB) promises to simplify the process. This article takes you into the underlying layers of what USB technology is all about. USB is a peripheral bus standard developed by PC and telecom industry leaders-Compaq, DEC, IBM, Intel, Microsoft, NEC and Northern Telecom-that brings the plug-and-play of computer peripherals outside the box, eliminating the need to install cards into dedicated computer slots and reconfigure the system. Personal computers equipped with USB allow computer peripherals to be automatically configured as soon as they are physically attached-without the need to reboot or run setup routines. USB also allows multiple devices (up to 127) to run simultaneously on a computer, with peripherals such as monitors and keyboards acting as additional plug-in sites or hubs.
Subfile: C

3/AB,3/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

5586470 INSPEC Abstract Number: B9707-0170L-005, C9707-5260B-049
Title: Automatic configuration of surface inspection systems
Author(s): Kueblbeck, C.; Wagner, T.
Author Affiliation: Fraunhofer Inst. fur Integrated Circuits, Erlangen, Germany
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3029 p.128-38
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1997 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1997)3029L.128:ACSI;1-O
Material Identity Number: C574-97111
U.S. Copyright Clearance Center Code: 0 8194 2440 4/97/$10.00
Conference Title: Machine Vision Applications in Industrial Inspection V
Conference Sponsor: SPIE; Soc. Imaging Sci. & Technol
Conference Date: 10-11 Feb. 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: Automatic image processing systems suffer from high engineering costs that are necessary to adapt the configuration of the system to the problem under consideration. As a consequence, this paper presents an approach to reduce these costs by applying optimization methods to the setup and the configuration of an image processing system. We report on experiments in which we automatically select adequate subsets of textural features from a large set of potential candidates. In addition, we tell how and why a training pattern selection is used as a part of the optimization process. Finally, we show how genetic programming can be used for the construction of new genetic feature sets. This method has no conventional counterpart and offers an interesting way to complement the algorithms made by humans.

services in a scalable, secure manner. This paper describes the I-WAY networking experiment, a large-scale wide-area computing testbed that has been used to investigate these issues. It also introduces the Globus project, a multi-institutional effort that is developing key technologies for I-WAY-like systems, including mechanisms for resource location, scheduling, authentication, and automatic configuration of high-performance distributed computations.
Subfile: B C

3/AB,3/24 (Item 24 from file: 2)
DIALOG(R)File 2:INSPEC

5437679 INSPEC Abstract Number: B9701-2250-005, C9701-7410D-075
Title: Using genetic algorithms to automate system implementation in a novel three-dimensional packaging technology
Author(s): Larcombe, S.P.; Prendergast, D.J.; Thacker, N.A.; Ivey, P.A.
Author Affiliation: Electron. Syst. Group, Sheffield Univ., UK
Conference Title: Proceedings. International Conference on Computer Design. VLSI in Computers and Processors (Cat. No.96CB36001) p.274-9
Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA
Publication Date: 1996 Country of Publication: USA xx+589 pp.
ISBN: 0 8186 7554 3 Material Identity Number: XX96-03376
U.S. Copyright Clearance Center Code: 1063-6404/96/$5.00
Conference Title: Proceedings International Conference on Computer Design. VLSI in Computers and Processors
Conference Sponsor: IEEE Comput. Soc. Tech. Committee on Design Autom.; IEEE Circuits & Syst. Soc.; IEEE Electron Devices Soc
Conference Date: 7-9 Oct. 1996 Conference Location: Austin, TX, USA
Language: English
Abstract: Implementing electronic systems in a low-cost, three-dimensional multichip module (MCM) technology provides significantly improved system density over planar packaging technologies. However, the extra dimension necessitates a new approach to design automation. Through experience gained in manually partitioning electronic systems, generic design rules have been formulated and implemented in software. The approach adopted is based on a genetic algorithm which can produce multiple candidate solutions and has the potential to simultaneously optimize multiple design criteria. This paper presents the initial results for the automatic configuration of a variety of systems. The results obtained by the algorithm are compared to known optimal solutions for "test" cases and to the results obtained by manual partitioning for the first heterogeneous MCM-V system.
Subfile: B C

3/AB,3/25 (Item 25 from file: 2)
DIALOG(R)File 2:INSPEC

5427342 INSPEC Abstract Number: B9701-6210L-008, C9701-6150N-008
Title: IPng: the next generation of the Internet Protocol
Author(s): Carpenter, B.
Author Affiliation: Commun. Syst. CN Div., CERN, Geneva, Switzerland
Journal: SWITCH Journal no.1 p.10-12
Publisher: Stiftung SWITCH,
Publication Date: 1995 Country of Publication: Switzerland
Material Identity Number: F312-96001
Language: English

load balancing and communication optimized process distribution onto arbitrary (network) topologies as well as efficient and secure routing strategies. A sophisticated performance analyser provides the system with the necessary load and communication cost information. MARC, which is realized so far for the language Occam and transputer networks, aims towards a true distributed operating system and development environment for parallel (MIMD) architectures. The paper outlines the features of MARC and describes in detail the mapping and routing strategies.
Subfile: C

3/AB,3/39 (Item 39 from file: 2)
DIALOG(R)File 2:INSPEC

03667905 INSPEC Abstract Number: C90046366
Title: Automatic configuration of transputer based systems
Author(s): Kramer, O.
Author Affiliation: Gesellschaft fur Math. und Datenverarbeitung mbH, St. Augustin, West Germany
Conference Title: Parallel Computing 89. Proceedings of the International Conference p.547-53
Editor(s): Evans, D.J.; Joubert, G.R.; Peters, F.J.
Publisher: North-Holland, Amsterdam, Netherlands
Publication Date: 1990 Country of Publication: Netherlands 630 pp.
ISBN: 0 444 88386-x
Conference Date: 29 Aug.-1 Sept. 1989 Conference Location: Leiden, Netherlands
Language: English
Abstract: In the second generation of transputer based systems, the links can be switched electronically. The author presents a tool for the automatic configuration. For a given process graph and a hardware description, MapTransputer computes a near-optimal multiprocessor configuration. Furthermore the placement of the processes and a shortest-path routing of the channels through this configuration are calculated. the structure and the algorithms used in the configuration tool are presented in this paper. The configuration tool is embedded into the programming environment SPECTRAL. SPECTRAL supports a hardware independent graphical specification of parallel software and overcomes the restrictions of transputer based systems. SPECTRAL generates a small and very efficient runtime system automatically only on the processors where needed.
Subfile: C

N/A

3/AB,3/40 (Item 40 from file: 2)
DIALOG(R)File 2:INSPEC

03258790 INSPEC Abstract Number: B88073654, C88063748
Title: Automatic configuration for fiber-based LANs
Author(s): Zurfluh, E.A.; Muller, H.R.
Author Affiliation: IBM Res. Div., Zurich Res. Lab., Ruschlikon, Switzerland
Conference Title: EFOC/LAN-88. Papers Presented at: The Sixth European Fibre Optic Communications and Local Area Networks Exposition. Proceedings p.408-13
Publisher: IGI Europe, Basel, Switzerland
Publication Date: 1988 Country of Publication: Switzerland xvi+483 pp.
Conference Date: 29 June-1 July 1988 Conference Location: Amsterdam, Netherlands
Language: English

--963

14728764 PASCAL No.: 00-0405140
PNNI Augmented Routing (PAR) and Proxy-PAR
HAAS R; DROZ P; BAUER D
Zurich Research Lab, Ruschlikon, Switzerland
Journal: Computer Networks, 2000, 34 (3) 399-418
Language: English

ATM networks are often used to carry IP traffic, but IP over ATM techniques suffer from complex and error-prone configuration. PNNI Augmented Routing (PAR) is an extension to PNNI to simplify IP support. In addition, a very lightweight interface called Proxy-PAR enables ATM-attached IP devices to operate without a full PAR implementation. PAR and Proxy-PAR provide a service discovery system for IP devices attached to ATM-PNNI networks. PAR and Proxy-PAR are standards from the ATM Forum, and are referenced by the IETF. This paper shows how PAR and Proxy-PAR can complement solutions, such as ILMI-based Server Discovery, Classical IP and ARP over ATM, and Next-Hop Resolution Protocol, or even replace existing solutions, for instance where a distributed address resolution mechanism is preferable to a centralized one. This is then described in the context of three different types of networks: a campus, a backbone, and a mobile network.

?rd s3
...completed examining records
S9 47 RD S3 (unique items)
?ds

Set	Items	Description
S1	20671	COMPUTER SYSTEM
S2	716519	CONFIGURATION
S3	49	AUTOMATIC CONFIGURATION
S4	1616269	STRUCTURAL
S5	0	S1 AND S3 AND S4
S6	0	S3 AND S4
S7	0	S1 AND S3
S8	0	S3 AND PD<930529
S9	47	RD S3 (unique items)

?

None applicable

LAK